Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.014”**

**G**

**S**

**D**

**2008**

**JP**

**202A**

**LS**

**.003”**

**.003”**

**.0043”**

**.020”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .003” min.**

**Backside Potential:**

**Mask Ref: JF202**

**APPROVED BY: DK DIE SIZE .014” X .020” DATE: 10/18/21**

**MFG: CALOGIC THICKNESS .013” P/N: 1N4118A**

**DG 10.1.2**

#### Rev B, 7/1